FULL TRANSLATION OF JAPANESE UNEXAMINED PATENT PUBLICATION (KOKAI) NO. 1-188043

Title of the Invention: Multiplex Converter

Publication Date: July 27, 1989

Patent Application No.: 63-9707

Filing Date: January 21, 1988

Applicants: Canon K.K.

2. SCOPE OF CLAIM FOR PATENT

1. A multiplex converter including a data storage section for storing data for at least the number of time slots in a frame, and transmitting the data stored in the data storage section in a time division multiplex system, said multiplex converter comprises:

reception means for receiving request for assignment of plural time slots from terminals;

search means for searching the idle state of time slots in response to said assignment request;

decision means for deciding the allowableness of the connection of said terminals based on the state of idleness of said time slots; and

assignment means for assigning plural time slots to said data storage portion in connection capable terminals.

2. A multiplex converter according to claim 1, wherein said search means include repetitive search means for repetitively searching by setting a predetermined waiting time, even when an idle time slot is not detected in the search.

3. DETAILED DESCRIPTION OF THE INVENTION

[Field of the Invention]

The present invention relates to a multiplex converter, and more particularly to a multiplex converter that performs communication in a time division multiplex system.

[Prior Art]

In recent years, apparatuses of this type have been increasingly employed for handling multi-media information directed to OA (Office Automation) equipments such as telephones, facsimiles, personal computers, and the like.

As a communication system for this purpose, in order to use one transmission line for data transmission in common by plural terminal equipments, a multiplex communication system is adopted in which a transmission line is multiplexed for communication. The multiplex communication system can be divided, for example, into two types, that is, a frequency division multiplex communication system in which multiplexing is performed on frequency axis and a time division multiplex communication system in which multiplexing is performed on time axis.

In the case of a time division multiplex communication system that adopts synchronizing method to assign a fixed length time slot to a terminal equipment at a regular period, one time slot in a frame is fixedly assigned to a connected terminal equipment. In order to increase the transmission volume in communication, the number of bits per time slot may be increased.

[Problem to be Solved by the Invention]

In the prior system as described above, transmission volume that can be transferred per unit time in communication is determined by the number of frames per unit time, leading to the problem that maximum transmission rate per terminal equipment is thereby limited.

In view of the conventional transmission rate, increasing the number of bits per time slot would give rise to the problem that idle bits may be produced in a time slot, and that total number of time slots to be positioned in a frame per unit time, hence number of terminal equipments which can be connected, may be thereby decreased.

[Means to Resolve the Problem]

In order to resolve the problem as described above and

to attain the object, a multiplex converter according to the present invention is a multiplex converter that includes a data storage section for storing data for at least the time slots in a frame, and transmits the data in the data storage section in a time division multiplex system, comprising, reception means for receiving request for assignment of plural time slots from terminal equipments; searching means for searching the idle state of time slots in response to said assignment request; determination means for determining the connection enable or disable state of said terminal equipments based on said idle state of time slots; and assignment means for assigning plural time slots to said data storage section of a connection enable terminal equipment.

[Operation]

With the construction as described above, the reception means receive request for assignment of plural time slots from terminal equipments, and the searching means search idle state of time slots. The determination means determine the connection enable or disable state of the terminal equipment based on the idle state of time slots. Based on this determination, the assignment means assign plural time slots to the data storage section of a connection enable terminal equipment.

In this manner, by allowing one terminal equipment to occupy plural time slots in a frame, it is possible to realize improved data communication in a time division multiplex communication system.

[Description of Preferred Embodiments]

Now, the present invention will be described in detail below with reference to appended drawings showing preferred embodiment thereof. A multiplex converter utilizing a time division multiplex system is used in this embodiment.

Figure 1 is a schematic block diagram showing the construction of a multiplex converter according to the present embodiment.

First, circuit construction of the reception system

according to the present invention will be described below.

In Fig. 1, reference numeral 1 denotes a multiplex converter of the present embodiment. Reference numeral 2 is a CPU for controlling the entire multiplex converter 1, reference numeral 3 is a ROM for storing a control program for CPU 1, an error processing program, a program for executing operation based on flow charts as shown in Figs. 4(a), 4(b) to be described later, and the like. Reference numeral 4 represents a RAM to be used as the work area for execution of various programs, a temporary data saving area in error processing, or the like.

The R_x is a time division multiplexed received signal sent from another multiplex converter having similar function as the multiplex converter of the present embodiment. Reference numeral 10 represents a reception circuit having demodulation function for converting the received signal R_x modulated in a particular signal system into binary digital signal, reference numeral 11 represents a reception buffer for temporarily storing the received data as converted into digital signal by the reception circuit 10. Reference numeral 12 represents a reception control circuit for controlling operation at the time of reception. The reception control circuit 12 comprises the time slot table as shown in Fig. 5 to be described later that stores the information as to which terminal equipment among those connected to the present converter a time slot in 1 frame is assigned.

Reference numeral 13 represents a distributing circuit that distributes received data to specified terminal equipments based on control signal in the time slot table contained in the reception control circuit 12. Reference numerals 14 ~ 17 represent reception storage circuits to which specified received data to be sent to various terminal equipments are input from the distributing circuit 13 and are stored.

The circuits of the reception system of the present

embodiment are constructed as described above.

Reference numerals 18 ~ 21 represent data exchange control circuits that perform the control for sending the received data stored in the reception data storage circuits 14 ~ 17 to the specified terminal equipments 40 ~ 42, and the control for sending the transmission data of the terminal equipments 40 ~ 42 to the specified storage circuits 22 ~ 25 to be described later.

The terminal equipment 40 that is to be provided with the function of a double unit communication speed is connected to both data exchange control circuits 18 and 19 in order to utilize two time slots for achieving the double unit communication speed. The terminal equipments 41 and 42 are to be provided with the function of a single unit communication rate, and in order to utilize one time slot, they are connected to the data exchange control circuits 20 and 21, respectively, in one-to-one correspondence to the respective time slots.

Next, the circuit construction of the transmission system of the present embodiment will be described below.

In Fig. 1, reference numerals 22 ~ 25 represent transmission storage circuits for storing transmission data received from the respective terminal equipments 40 ~ 42, reference numeral 28 represents a transmission control circuit for controlling operation at the time of transmission. The transmission control circuit 28 comprises the time slot table as described before that stores the information as to which terminal equipment among the terminal equipments 40 ~ 41 connected to the present converter each time slot in one frame is assigned. Reference numeral 26 represents a multiplexing circuit for loading respective transmission data stored in the transmission storage circuits 22 ~ 25 to the specified time slots by the control signal based on the time slot table contained in the transmission control circuit 28. As used herein, "loading to the time

slot" means assigning transmission data to the specified time position and sending out the same.

Reference numeral 27 represents a transmission buffer for temporarily storing prescribed transmission data that has been multiplexed in the multiplexing circuit 26. Reference numeral 29 represents a transmission circuit having modulation function for converting the transmission data, that is, binary digital signal, stored in the transmission buffer 27 into a particular signal system, and T_x is the transmission signal that has been time division multiplexed in the multiplexing circuit 26 to be transmitted from the transmission circuit 29 to a multiplex converter having similar function as the multiplex converter of the present invention.

Reference numeral 30 represents a slot assignment control circuit that sends out the control signal such as updating of above described time slots or the like to the reception control circuit 12 and to the transmission control circuit 28, and performs updating of the time slot table or the like. The slot assignment is performed based on the slot assignment control signal from various connected terminal equipments.

Next, the control procedure for slot connection/release performed by the multiplex converter 1 of the present embodiment will be described.

Figure 2(a) is a flow chart showing steps of a connection request processing for obtaining slots in response to connection request from a terminal equipment, and FIG. 2(b) is a flow chart showing steps of a release request processing for releasing slots in response to release request from a terminal equipment. Figure 3 is a view useful for explaining the time slot table of the present embodiment.

First, the connection request processing is described with reference to Fig. 2(a).

When a connection request is received from a terminal equipment, parameters such as the number of requesting

terminal equipment, respective quantity of the transmission storage circuit 14 ~ 17 and the reception storage circuit 22 ~ 25 for transmission to/reception from the terminal equipment, respective physical position number of the reception buffer 11 and the transmission buffer 27 connected to the distributing circuit 13 and multiplexing circuit 26, reservation number of slots, and the like are received and set to the prescribed buffer of the CPU 1 (step S1).

Then, maximum number of retrial is set (step S2). As used herein, "retrial" means a processing in which, if no idle slot cannot be detected in a search, an idle slot is searched again after a predetermined time period, and "maximum number" means the maximum number of searching trials.

Here, the time slot table for time slots controlled by the reception control circuit 12 and transmission control circuit 28 will be explained below with reference to FIG. 3.

In the figure, the time slot table is constructed with prescribed memory elements. In the vertical direction of the table, the slot No. is indicated from No. 1 to No. n. The slot No. indicates the address of each memory element, and specified data are stored at the position of this address. In the horizontal direction, bits b_0 ~ b_5 store the physical position number of the transmission storage circuit or the reception storage circuit that is using the slot, and bit b_6 is a reservation bit and bit b_7 is a busy bit, respectively. In this manner, slot data of 8 bits consisting of bits b_0 ~ b_7 are used in the present embodiment.

For example, when the busy bit indicates the flag "1", the slot with the slot No. is a slot being used. On the other hand, the busy bit with the flag "0" indicates an idle slot. When the reservation bit indicates the flag "1", the slot of that slot No. is the slot being reserved, while the flag "0" indicates an unreserved, idle slot.

Next, based on the maximum number of searching for an idle slot that has been set at step S1, an idle slot is

searched successively from slot No. 1 to No. n of the above described time slot table (step S3). If an idle slot is detected, the process moves to step S5 (step S4). If all the slots are being used, searching operation is repeated for the maximum number of retrial. In this case, the number of retrial is first decremented by one (step S5, step S6), and after waiting for a predetermined period (step S7), the process returns to step S3 to repeat the searching operation.

Waiting for a predetermined period at step S7 is a processing necessary in order to perform searching of an idle slot with a finite time interval. If an idle slot is searched without this waiting time, probability of successfully finding an idle slot would be low. Thus, by setting a predetermined waiting time in order to allow for sufficient time in release processing in which a slot being used by other terminal equipment is released, the probability of finding an idle slot may be increased.

If an idle slot is found at step S4, the reservation bit of that slot No., or the address position, is set to "1", and the physical position number is stored in the bits b_0~ b_5 of the table (step S8).

Since a multi-slot system is adopted in the present embodiment, plural slots need to be obtained. Therefore, reservation processing is necessary in order to check whether or not all the required number of slots can be secured, or whether or not there are required number of idle slots.

After an idle slot is reserved at step S8, reservation number of slots is incremented by one to count up the reservation number (step S9).

This counting of reservation number may be performed either in count-up method or in count-down method. Count-up method is adopted in the present embodiment. Therefore, the initial value is set to "0" when setting parameters at step S1.

Then, it is determined whether or not the required number of slots as requested from the terminal equipment have

been secured, and if the required number of reserved slots have not been secured, processing from step S1 to step S9 is repeated (step S10).

On the other hand, if all the required number of slots have been secured, the flag of the busy bit of the reserved slot is set to "1", and the reservation is thereby definitely set (step S11). Then, the reservation number that has been counted up at step S9 is counted down by decrementing the number by one(step S12), and processing at step S11 and step S12 is repeated until all the flags of the busy bits of slots reserved at step S8 have been set to "1" (step S13).

When reservation of slots has been definitely completed in this manner, the terminal equipment that sent the connection request is informed of the completion of the slot acquisition, and the connection processing to the terminal equipment is terminated (step S14).

This step S14 is a process of sending out an ACK (acknowledge) that has the purpose of informing the terminal equipment of the successful acquisition of slots.

If no idle slot can be found at step S4, the next retrial processing is performed.

If the maximum number of retrial has not been completed, processing at step S6 and step S7 as described above may be performed. If the maximum number of retrial has been completed, a processing is performed in which all the reservation bits of reserved slots are released. This is the slot release processing in the case where the retrial processing cannot find an idle slot.

When, in the determination of retrial number at step S5, the number of retrial comes to the set upper limit, it indicates a failure in the acquisition of slots.

In order to release the reserved slots, the flag of the reservation bit of the reserved slot is reset to "0" (step S14), and the reservation number is decremented by one for count-down (step S16). In this manner, all the reserved slots are released one by one beginning from the slot with

earlier slot No. (step S17).

When all the reserved slots have been released in this manner, the failure of the acquisition of slots is informed as a NACK (negative acknowledge) sent out to the terminal equipment. This constitutes the connection disable notice to the terminal equipment.

Based on the foregoing explanation, for example, with reference to the time slot table as shown in Fig. 3, in the case of the slots No. 1 and No. 2, it indicates that the slots are being used, while in the case of the slots No. 3 and No. n, it indicates that the slots are idle. In the case of the slots No. (n-m) and No. (n-1), it indicates that the slots are being reserved.

Next, a release processing in which slots are released in response to release request from a terminal equipment will be described below with reference to Fig. 2(b).

In the same manner as in a connection request processing described above with reference to Fig. 2(a), parameters (the number of the terminal equipment, number of transmission and reception storage circuits, physical position number, and the like) are received and stored in the prescribed buffer of the CPU 1 (step S100).

When reception of various parameters have been completed, the flag of the busy bit of the slot is set to "0" and the slot is released (step S101). Release of slots is repeated until the number of slots comes to the number of indirect connection of connected transmission and reception storage circuits (step S102 ~ step S104).

When the number of released slots comes to the number of connected slots, an ACK (acknowledge) indicating the completion of slot release is sent out to the terminal equipment, which constitutes the notice of the release of connection to the terminal equipment.

In the present embodiment, the transmission storage circuit and the reception storage circuit are each provided with one time slot table, respectively. The present

invention, however, is not limited to this construction, and one time slot table that can be shared by both circuits may be utilized.

Next, the communication method in a time division multiplex system according to the present embodiment will be explained by way of an example.

Figure 4 is a block diagram showing the construction of the connection between multiplex converters according to the present embodiment.

In Fig. 4, 11, 11' are multiplex converters having similar function as the multiplex converter 1 of the present embodiment, comprising a greater number of unshown data exchange control circuits and transmission- and reception storage circuits than the multiplex converter 1. The multiplex converter 11 has terminals 50 - 52 connected thereto, and the multiplex converter 11' has terminals 53 ~ 55 connected thereto, respectively. In this manner, data communication in the time division multiplex system according to the present embodiment is performed via the data transmission line 31 that is connected between the multiplex converters.

Next, referring to Fig. 4, the time division multiplex system of the present embodiment in which data are transmitted from the terminal 50 to the terminal 53, from the terminal 51 to the terminal 54, and from the terminal 52 to the terminal 55, will be explained below.

Figure 5 is a schematic view for explaining the time division multiplex system according to the present embodiment, and Fig. 6 is a schematic view for explaining the prior time division multiplex system.

As shown in Fig. 5, characters "1" ~ "3" are transmitted between the terminal 50 and the terminal 53, characters "A" ~ "C" are transmitted between the terminal 51 and the terminal 54, and characters "i (Japanese)" - "ro (Japanese)" are transmitted between the terminal 52 and the terminal equipment 55, in the time division multiplex system.

First, when transmitting, the multiplex converter 11 assigns one time slot to the character "1" of the terminal 50, and assigns one time slot to each of the characters "A" and "B" of the terminal 51 with greater amount of information. The terminal 52 has also greater amount of information, and one time slot is assigned to each of the characters "i (Japanese)" and "ro (Japanese)". The first frame is composed in this manner.

Also in the composition of the second and third frame, in the case of the terminal equipments 51 and 52, two time slots are assigned to the characters constituting the transmission data.

When data are transmitted in this manner to the terminals 53 - 55 on the reception side, the multiplex converter 11' sends out the character "1" to the terminal 53, the characters "A" and "B" to the terminal 54, and the characters "i (Japanese)" and "ro (Japanese)" to the terminal 55, respectively.

Thus, the terminals 51 and 54, and the terminals 52 and 55, respectively, can communicate with each other with double amount of information contained in one frame so that the transmission rate is twice as great as the ordinary transmission rate. It is to be understood that the amount of data transmitted per unit time can be increased by increasing the number of assigned time slots in one frame, and the transmission rate can be increased accordingly.

In the prior system, as shown in Fig. 6, between a pair of terminals (that is, between the terminals 56 and 59, between the terminals 57 and 60, and between the terminals 58 and 61), data being transmitted in the transmission line 32 occupy only one time slot fixedly positioned in the first to the third frames as shown between the synchronized signals.

The multiplex converter according to the present embodiment will be compared below with the prior multiplex converter. With the multiplex converter according to the present embodiment, the 6 characters "A" ~ "F" transmitted

from the terminal 51, and the 6 characters "i (Japanese)" ~ "ro (Japanese)" transmitted from the terminal 52, can be transmitted in the first to the third frames.

On the other hand, with the prior multiplex converter, by the transmission in the first to the third frames, only the characters "1" ~ "3" between the terminal equipments 56 and 59, only the characters "A" ~ "C" between the terminals 57 and 60, and only the characters "i (Japanese)" ~ "ro (Japanese)" between the terminals 58 and 61, respectively, can be transmitted.

Thus, in the prior system, the upper limit of the amount of data transmission per unit time is determined by the number of frames transmitted per unit time. Therefore, in the prior time division multiplex communication system, a terminal that exceeds this upper limit of transmission rate could not be connected.

In this manner, the problem associated with the prior multiplex system as shown in Fig. 6 can be satisfactorily resolved with the multiplex converter according to the present embodiment by increasing the number of assigned time slots.

As has been described above, in accordance with the present embodiment, amount of transmission can be increased and communication speed can be considerably improved by assigning plural time slots in one frame in the time division multiplex system to a terminal with high communication speed or having greater amount of data transmission.

Since the amount of data transmission and the communication speed depend only on the number of assigned time slots in one frame, the multiplex converter can easily accommodate terminals with different amounts of transmission or different communication speeds.

[Effect of the Invention]

As has been described above, in accordance with the present invention, amount of transmission can be increased and communication speed can be improved by assigning plural

time slots in one frame to the terminal.

4. BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic block diagram useful for explaining the construction of a multiplex converter according to the present embodiment;

Figs. 2(a) and 2(b) are flow charts showing the time division multiplex system of the present embodiment;

Fig. 3 is a view useful for explaining the time slot table according to the present embodiment;

Fig. 4 is a block diagram showing the construction of the connection between multiplex converters according to the present embodiment;

Fig. 5 is a schematic view useful for explaining the time division multiplex system according to the present embodiment; and

Fig. 6 is a schematic view useful for explaining the prior time division multiplex system.

[Reference Numerals]

1, 11, 11', 100, 100'----multiplex converter,
2----CPU,
3----ROM,
4----RAM,
10----receiving circuit,
11----reception buffer,
12----reception control circuit,
13----distributing circuit,
14 ~ 17----reception storage circuit,
18 ~ 21----data exchange control circuit,
22 ~ 25----transmission storage circuit,
26-----multiplexing circuit,
27-----transmission buffer,
28----transmission control circuit,
29----transmission circuit,
30----slot assignment control circuit,

50 - 61----terminal